Interface techniques for embedding custom mega cells in a gate array

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References Cited: 1
Accession Number: 4972454

Abstract:

A full custom microprocessor mega cell is embedded in a 0.7-micron triple-layer metal gate array using shrinkable design rules. Interface logic built from gate array macros guarantees data sheet timing at the pins, production test pattern transportability, and CRC/BIST (cyclic redundancy check/built-in self-test) testability. The processor was modeled using behavioral Verilog wrapped around proprietary 'C' code.

Subject Terms:

microprocessor chips; BIST testability; ASIC; simulation; cyclic redundancy check testability; C model; interface logic; timing verification; embedding; full custom; microprocessor mega cell; triple-layer metal gate array; shrinkable design rules; gate array macros; data sheet timing; production test pattern transportability; behavioral Verilog; 0.7 micron

Block diagram compilation and graphical editing of DSP algorithms in the QuickSig system

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This Paper Appears in :
Circuits and Systems, 1988., IEEE International Symposium on

on Pages: 1057 - 1060 vol.2

This Conference was Held : 7-9 June 1988
1988
Total Pages: 3 vol. 2915
References Cited: 8
Accession Number: 3327105

Abstract:

The QuickSig system is an experimental integrated software environment for digital signal processing, based on the use of the Common Lisp language and object-oriented programming. The authors describe the approach of using a block diagram compiler and an interactive graphical editor in digital signal processor software development. The object-oriented approach on the Common Lisp language is well suited to the problem due to its flexibility in terms of manipulating symbolic expressions and object structures. The system compiles an efficient Lisp code from block diagram descriptions and is able to use different strategies and styles of code generation. Possible extensions to the system, e.g. the generation of code for signal processor chips, are also discussed.<>

Subject Terms:

An architecture for electrically configurable gate arrays

- *El Gamal, A.; Greene, J.; Reyneri, J.; Rogoyski, E.; El-Ayat, K.A.; Mohsen, A.*
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This Paper Appears in :
Solid-State Circuits, IEEE Journal of

on Pages: 394 - 398

April 1989 Vol. 24 Issue: 2 ISSN: 0018-9200
References Cited: 6
CODEN: IJSCBC
Accession Number: 3420744

Abstract:

An architecture for electrically configurable gate arrays using a two-terminal antifuse element is described. The architecture is extensible, and can provide a level of integration comparable to mask-programmable gate arrays. This is accomplished by using a conventional gate array organization with rows of logic modules separated by wiring channels. Each channel contains segmented wiring tracks. The overhead needed to program the antifuses is minimized by an addressing scheme that utilizes the wiring segments, pass transistors between adjacent segments, shared control lines, and serial addressing circuitry at the periphery of the array. This circuitry can also be used to test the device prior to programming and observe internal nodes after programming. By providing sufficient wiring tracks segmented into carefully chosen lengths and a logic module with a high degree of symmetry, fully automated placement and routing is facilitated.<>

Subject Terms:

automated routing; CMOS; electrically configurable gate arrays; two-terminal antifuse element; level of integration; gate array

An architecture for a DSP field-programmable gate array

- *Agarwala, M.; Balsara, P.T.*
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This Paper Appears in :
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

on Pages: 136 - 141

March 1995 Vol. 3 Issue: 1 ISSN: 1063-8210
References Cited: 6
CODEN: IEVSE9
Accession Number: 4915497

Abstract:

This paper describes an application specific architecture for field-programmable gate arrays (FPGAs). Emphasis is placed on the logic module architecture and channel segmentation for the FPGAs targeted for application areas related to digital signal processing (DSP). The proposed logic module architecture is well-suited for efficient implementation of frequently used logic functions in the DSP application area. This is mainly because it is possible to implement most of these functions using one logic module, which results in a reduction in both the net lengths and the number of antifuses used. The performance improvements are achieved by customizing the logic module architecture and the programmable interconnect to suit the requirements of DSP applications.<>

Subject Terms:

field programmable gate arrays; programmable logic arrays; application specific integrated circuits; digital signal processing chips; DSP

Routing architectures for hierarchical field programmable gate arrays

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Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedings., IEEE International Conference on

on Pages: 475 - 478

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1994 ISBN: 0-8186-6565-3
IEEE Catalog Number: 94CH35712
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References Cited: 13
Accession Number: 4801116

Abstract:

This paper evaluates an architecture that implements a hierarchical routing structure for FPGAs, called a hierarchical FPGA (HFPGA). A set of new tools has been used to place and route several circuits on this architecture, with the goal of comparing the cost of HFPGAs to conventional symmetrical FPGAs. The results show that HFPGAs can implement circuits with fewer routing switches, and fewer switches in total, compared to symmetrical FGPAs, although they have the potential disadvantage that they may require more logic blocks due to coarser granularity.<>

Subject Terms:

network routing; logic arrays; logic design; circuit diagrams; circuit switching; hierarchical field programmable gate arrays; routing